CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is as follows:

1. A process of testing spacing of wiring in a circuit comprising:

forming a plurality of conductor rectangles representative of conductors of said circuit;

forming minimum spacing rectangles around said conductor rectangles, said minimum spacing rectangles being larger than respective ones of said conductor rectangles;

identifying a possible error rectangle when a first conductor rectangle of said conductor rectangles occupies a portion of a minimum spacing rectangle of a second conductor rectangle of said conductor rectangles;

checking whether said possible error rectangle is a true error; and

reporting said true errors.

2. The process in claim 1, wherein said checking comprises:

classifying said possible error rectangle as a possible diagonal error rectangle or a possible non-diagonal error rectangle;

determining that said possible diagonal error rectangle is said not a true error when at least two adjacent sides of said possible diagonal error rectangle

which connect said first conductor and said second conductor are covered by a third conductor of said conductors; and

determining that said possible non-diagonal error rectangle is not a true error when said possible non-diagonal error rectangle is completely covered by said third conductor.

3. The process in claim 1, wherein said forming minimum spacing rectangles comprises forming said minimum spacing rectangles to have sides which are a minimum spacing design constraint distance from sides of respective ones of said conductor rectangles.

4. The process in claim 1, wherein said conductors are within a single net.

5. The process in claim 1, wherein said circuit comprises a plurality of nets and said process further includes checking for shorts between different ones of said nets.

6. The process in claim 1, further comprising dividing said possible error rectangle into at least two possible error rectangles if said possible error rectangle is partially covered by a third conductor of said conductors.

7. A process of testing spacing of elements in a structure comprising:

forming a plurality of element rectangles representative of elements of said structure;

forming minimum spacing rectangles around said element rectangles, said minimum spacing rectangles being larger than respective ones of said element rectangles;

identifying a possible error rectangle when a first element rectangle of said element rectangles occupies a portion of a minimum spacing rectangle of a second element rectangle of said element rectangles;

checking whether said possible error rectangle is a true error; and

reporting said true errors.

8. The process in claim 7, wherein said checking comprises:

classifying said possible error rectangle as a possible diagonal error rectangle or a possible non-diagonal error rectangle;

determining that said possible diagonal error rectangle is said not a true error when at least two adjacent sides of said possible diagonal error rectangle which connect said first element and said second element are covered by a third element of said elements; and

determining that said possible non-diagonal error rectangle is not a true error when said possible non-diagonal error rectangle is completely covered by said third element.

9. The process in claim 7, wherein said forming minimum spacing rectangles comprises forming said minimum spacing rectangles to have sides which are a minimum spacing design constraint distance from sides of respective ones of said element rectangles.

10. The process in claim 7, wherein said elements are within a single net.

11. The process in claim 7, wherein said structure comprises a plurality of nets and said process further includes checking for shorts between different ones of said nets.

12. The process in claim 7, further comprising dividing said possible error rectangle into at least two possible error rectangles if said possible error rectangle is partially covered by a third element of said elements.

13. A computer system for testing spacing of wiring in a circuit comprising:

a unit for forming a plurality of conductor rectangles representative of conductors of said circuit;

a unit for forming minimum spacing rectangles around said conductor rectangles, said minimum spacing rectangles being larger than respective ones of said conductor rectangles;

a unit for identifying a possible error rectangle when a first conductor

rectangle of said conductor rectangles occupies a portion of a minimum spacing rectangle of a second conductor rectangle of said conductor rectangles;

a unit for checking whether said possible error rectangle is a true error; and

a unit for reporting said true errors.

14. The computer system in claim 13, wherein said unit for checking comprises:

a unit for classifying said possible error rectangle as a possible diagonal error rectangle or a possible non-diagonal error rectangle;

a unit for determining that said possible diagonal error rectangle is said not a true error when at least two adjacent sides of said possible diagonal error rectangle which connect said first conductor and said second conductor are covered by a third conductor of said conductors; and

a unit for determining that said possible non-diagonal error rectangle is not a true error when said possible non-diagonal error rectangle is completely covered by said third conductor.

15. The computer system in claim 13, wherein said unit for forming minimum spacing rectangles comprises a unit for forming said minimum spacing rectangles to have sides which are a minimum spacing design constraint distance from sides of respective ones of said conductor rectangles.

16. The computer system in claim 13, wherein said conductors are within a single net.

17. The computer system in claim 13, wherein said circuit comprises a plurality of nets and said computer system further includes a unit for checking for shorts between different ones of said nets.

18. The computer system in claim 13, further comprising a unit for dividing said possible error rectangle into at least two possible error rectangle if said possible error rectangle is partially covered by a third conductor of said conductors.

19. A computer program product comprising a program storage device readable by a computer system tangibly embodying a program of instructions executed by said computer system to perform a process for testing spacing of wiring in a circuit, said process comprising:

forming a plurality of conductor rectangles representative of conductors of said circuit;

forming minimum spacing rectangles around said conductor rectangles, said minimum spacing rectangles being larger than respective ones of said conductor rectangles;

identifying a possible error rectangle when a first conductor rectangle of said conductor rectangles occupies a portion of a minimum spacing rectangle of a second conductor rectangle of said conductor rectangles;

checking whether said possible error rectangle is a true error; and

reporting said true errors.

20. The computer program product in claim 19, wherein said checking comprises:

classifying said possible error rectangle as a possible diagonal error rectangle or a possible non-diagonal error rectangle;

determining that said possible diagonal error rectangle is said not a true error when at least two adjacent sides of said possible diagonal error rectangle which connect said first conductor and said second conductor are covered by a third conductor of said conductors; and

determining that said possible non-diagonal error rectangle is not a true error when said possible non-diagonal error rectangle is completely covered by said third conductor.

21. The computer program product in claim 19, wherein said forming minimum spacing rectangles comprises forming said minimum spacing rectangles to have sides which are a minimum spacing design constraint distance from sides of respective ones of said conductor rectangles.

22. The computer program product in claim 19, wherein said conductors are within a single net.

23. The computer program product in claim 19, wherein said circuit comprises a plurality of nets and said process further includes checking for shorts between different ones of said nets.

24. The computer program product in claim 19, said process further comprising dividing said possible error rectangle into at least two possible error rectangle if said possible error rectangle is partially covered by a third conductor of said conductors.